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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/578,380	01/22/2007	Takashi Hasunuma	YH0018-US1	6606

27788 7590 12/18/2008

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EXAMINER	
MURALIDAR, RICHARD V	
ART UNIT	PAPER NUMBER
2838	
MAIL DATE	DELIVERY MODE
12/18/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/578,380	HASUNUMA ET AL.	
	Examiner	Art Unit	
	RICHARD V. MURALIDAR	2838	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 May 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/17/2008*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

The IDS dated 11/17/2008 is not in conformance 37 CFR § 1.98. US Patent numbers should to be typed, along with their publication dates and inventors listed in the appropriate columns. The hand-typed numbers missing publication dates and inventors have not been considered.

Drawings

The drawings are objected to. Figure 4 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-3, 5-6, and 10-11 are rejected under 35 U.S.C. 102(e) as being anticipated by Ikeda, Patent No. 6,963,477.

With respect to claim 1, Ikeda discloses an overheat protection device [Fig. 1] comprising a variable resistive element [Fig. 1; PTC1] for of which resistance varies depending on a temperature, characterized in that the device further comprises a switching element [Fig. 1; 11; transistor Tr0] which controls a current flowing through an electrical system [Fig. 1; power supply 13] depending on an applied voltage thereto [col. 4 lines 59 – col. 5 lines 6], and the variable resistive element [Fig. 1, PTC1] is located on and thermally combined with a certain position of the electrical system [Fig. 1; power supply 13] and interrupts the current flowing through the electrical system by changing the applied voltage to the switching element when the certain position comes to be under a high temperature condition [col. 5 lines 6 – col. 7 lines 20].

With respect to claim 2, Ikeda disclose that the electrical system comprises a secondary battery [Fig. 2; power supply 13 is a battery; col. 4 lines 56-58], and the variable resistive element [Fig. 1; PTC1] is located on and thermally combined with the secondary battery.

With respect to claim 3, Ikeda discloses that the variable resistive element is a PTC element [Fig. 1; PTC1 element; col. 5 lines 7-9].

With respect to claim 5, Ikeda further comprises a resistor [Fig. 1; R2], the variable resistive element [Fig. 1; PTC1] and the resistor [Fig. 1; R2] are electrically connected in series with each other and in parallel to the electrical system [Fig. 1; PTC1 and R2 are in parallel with the power supply 13], and the switching element [Fig. 1; Tr0, Tr1] is electrically connected in parallel to the resistor.

With respect to claim 6, Ikeda discloses that the switching element [Fig. 1; transistors Tr0 and Tr1] is a field effect transistor (FET) [col. 8 lines 62-65], a gate of the FET is electrically connected to a position between the variable resistive element and one end of the resistor [Fig. 1; the gate of transistor Tr0 is connected between the PTC1 and resistor R2], a source of the FET is electrically connected to another end of the resistor [Fig. 1; source of transistor Tr0 is connected to another end of resistor R2 via PTC1], the source and a drain of the FET are electrically connected to form a part of an electric circuit comprising the electrical system [Fig. 1; the source and the drain of transistor Tr0 are electrically connected], and when a voltage between the gate and the source of the FET [Fig. 1; transistor Tr0] becomes not greater than a threshold value, the current does not substantially flow between the source and the drain of the FET so that the current flowing through the electrical system is interrupted [this is the normal operation of the transistor].

With respect to claim 10, Ikeda discloses an electrical system comprising the overheat protection device according to claim 1 [col. 1 lines 5-10].

With respect to claim 11, Ikeda discloses that the electrical system comprises a secondary battery [Fig. 1; power supply 13; col. 4 lines 56-58] which is electrically connected to an electrical element [Fig. 1; source and drain of transistor Tr0] to form an electric circuit, and the overheat protection device [Fig. 1; PTC1 and resistors R1, R2] is connected in parallel to and between the secondary battery and the electrical element [as shown in Fig. 1].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeda, Patent No. 6,963,477.

With respect to claim 4, Ikeda discloses that the variable resistive element is a PTC element, but does not disclose that the variable resistive element is composed of plural variable resistive elements, which are electrically connected in series with each other.

However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have provided the circuit with a plurality of variable resistive elements for the purpose of redundancy, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. St. Regis Paper Co. v. Bemis Co., 193 USPQ 8.

With respect to claim 7, Ikeda discloses that a value of the voltage between the gate and the source is expressed as a following formula (1): Vgs = Vo * (R/(P+R)); wherein the Vgs is the voltage between the gate and the source, the V0 is a voltage across the variable resistive element and the resistor, the P is a resistance of the variable resistive element, and the R is a resistance of the resistor [This is the standard voltage divider formula for calculating voltage across the gate and the source of the

transistor. One of ordinary skill in the art would know how to apply to Fig. 1 of Ikeda in order to determine the applicable Vgs].

Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeda, Patent No. 6,963,477, in view of Furuta et al., Patent No. 6,661,633.

With respect to claim 8, Ikeda does not disclose that the device further comprises another variable resistive element to prevent overcurrent in the electrical system.

Furuta discloses protective device for a battery [col. 1 lines 24-30], which comprises a variable resistive element [Fig. 2; 1] for which resistance varies depending on a temperature in order to prevent overcurrent in the electrical system [Fig. 1; battery terminals A1 and A2; col. 3 lines 64 - col. 4 lines 8].

Ikeda and Furuta are analogous battery protection circuits. It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate Furuta's PTC element, into Ikeda's overheat protection circuit, for the benefit of protecting the circuit from any other sources of excess temperature, such as over currents resulting from short circuits or overloads.

With respect to claim 9, Furuta discloses that the other variable resistive element is a PTC element [Fig. 2; PTC 1].

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to RICHARD V. MURALIDAR whose telephone number is (571)272-8933. The examiner can normally be reached on 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Akm E. Ullah can be reached on 571-272-2361. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Akm Enayet Ullah/
Supervisory Patent Examiner, Art Unit 2838

/Richard V Muralidar/
Examiner, Art Unit 2838